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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,640	03/17/2004	Kun-Hong Chen	ADTP0116USA	2639

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EXAMINER
NGUYEN, DAO H

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,640	CHEN, KUN-HONG	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the communications dated 03/17/2004 through 05/18/2004, claims 1-15 are active in this application.

Foreign Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

3. The specification has been checked to the extent necessary to determine the presence of possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim(s) 1-2 and 4-15 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,558,993 to Ohtani et al.

Regarding claim 1, Ohtani discloses a thin-film transistor, as shown in figs. 1A, 4B, comprising:

a substrate 101;

a semiconductor layer (col. 9, lines 13-18) positioned on the substrate 101, the semiconductor layer comprising a channel region 104, two lightly doped drains 108, and two source/drain regions 109; and

a gate 105 positioned on the substrate 101, the two lightly doped drains 108 being symmetrically arranged with respect to the gate 105, either of the two gate edges being

overlapped with the adjacent lightly doped drain 108, neither of the junctions between the lightly doped drains 108 and the source/drain regions 109 being overlapped with the gate 105, and neither of the source/drain regions 109 being overlapped with the gate 105. See also col. 9, line 13 to col. 11, line 23.

Regarding claim 2, Ohtani discloses the thin-film transistor wherein the gate 105 is positioned above the semiconductor layer. See figs. 1, 4.

Regarding claim 4, Ohtani discloses the thin-film transistor further comprising an insulating layer 103 positioned between the gate 105 and the semiconductor layer. See figs. 1, 4.

Regarding claim 5, Ohtani discloses the thin-film transistor wherein the substrate comprises a glass substrate. See col. 4, line 59.

Regarding claim 6, Ohtani discloses the thin-film transistor wherein the gate 105 comprises a length A (of 0.1- 10μm, col. 5, lines 60-62), the channel region 104 comprises a length B, the lightly doped drains 108 comprise a length C (of 0.2 – 4μm, col. 9, lines 52-65) (in addition, according to figs. 1 and col. 9, lines 52-65, channel length would be B = A-C), and a correlation among these lengths is as following:

$$B+0.2C \leq 0.5A \leq B+0.8C$$

for at least at the point where A = 5μm, C = 3.5μm, and B = A-C = 1.5μm. Specifically,

- B + 0.2C = 1.5 + 0.2*3.5 = 2.2μm;
- B + 0.8C = 1.5 + 0.8*3.5 = 4.3μm; and
- 0.5A = 0.5* 5 = 2.5μm

Then, the expression $B+0.2C \leq 0.5A \leq B+0.8C \Leftrightarrow 2.2 \leq 2.5 \leq 4.3$ is satisfied.

Regarding claim 7, Ohtani discloses the thin-film transistor wherein the lightly doped drains 108 have an equal length. See figs. 1.

Regarding claim 8, Ohtani discloses the thin-film transistor wherein a length of the lightly doped drains 108 is approximately between (0.3-3.5)μm. See col. 9, lines 57-59.

Regarding claim 9, Ohtani discloses a thin-film transistor, as shown in figs. 1, 4, comprising:

a substrate 101;

a semiconductor layer (col. 9, lines 13-18) positioned on the substrate 101, the semiconductor layer comprising a channel region 104, two lightly doped drains 108, a source 109 and a drain 109;

an insulating layer 103 positioned on the semiconductor layer; and

a gate 105 positioned on the insulating layer 103, the gate 105 comprising a gate edge (left edge) overlapped with the lightly doped drain 108 adjacent to the drain 109, the gate 105 being not overlapped with the junction between the lightly doped drain 108 and the drain 109, and the gate 1085 being not overlapped with the drain 109. See also col. 9, line 13 to col. 11, line 23.

Regarding claim 10, Ohtani discloses the thin-film transistor wherein the gate 105 comprises another gate edge (right edge) overlapped with the lightly doped drain 108 adjacent to the source 109, but the gate 105 is not overlapped with the junction between

the lightly doped drain 108 and the source 109, and the gate is 105 not overlapped with the source 109. See figs. 1-4.

Regarding claim 11, Ohtani discloses the thin-film transistor wherein the substrate comprises a glass substrate. See col. 4, line 59.

Regarding claim 12, Ohtani discloses the thin-film transistor wherein the gate 105 comprises a length A (of 0.1- 10μm, col. 5, lines 60-62), the channel region 104 comprises a length B, the lightly doped drains 108 adjacent to the drain comprise a length C (of 0.2 – 4μm, col. 9, lines 52-65) (in addition, according to figs. 1 and col. 9, lines 52-65, channel length would be B = A-C), and a correlation among these lengths is as following:

$$B+0.2C \leq 0.5A \leq B+0.8C$$

for at least at the point where A = 5μm, C = 3.5μm, and B = A-C = 1.5μm.

Specifically,

- B + 0.2C = 1.5 + 0.2*3.5 = 2.2μm;
- B + 0.8C = 1.5 + 0.8*3.5 = 4.3μm; and
- 0.5A = 0.5* 5 = 2.5μm

Then, the expression $B+0.2C \leq 0.5A \leq B+0.8C \Leftrightarrow 2.2 \leq 2.5 \leq 4.3$ is satisfied.

Regarding claim 13, Ohtani discloses the thin-film transistor wherein the lightly doped drains 108 have an equal length. See figs. 1.

Regarding claim 14, Ohtani discloses the thin-film transistor wherein a length of the lightly doped drains 108 is approximately between 0.3-3.5μm. See col. 9, lines 57-59.

Regarding claim 15, Ohtani discloses the thin-film transistor wherein the lightly doped drains are symmetrically arranged with respect to the gate. See figs. 1-4.

Claim Rejections - 35 U.S.C. § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim(s) 3 is rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,558,993 to Ohtani et al., in view of Yeh et al.

Regarding claim 3, Ohtani discloses the thin-film transistor comprising all claimed limitations, except for the gate being positioned below the semiconductor layer.

Yeh discloses a thin film transistor, as shown in figs. 1-2, comprising a semiconductor layer 22 having source/drain regions 27/28 and a channel therebetween. The thin film transistor of Yeh also has a buried gate electrode 25 positioned below the semiconductor layer 22.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Ohtani so that its gate electrode being a buried gate electrode as that of Yeh (such buried gate transistor is also very common in the art) in order to obtain a device with lower standby current, improved cell stability, and higher soft-error immunity (see col. 1, lines 12-17). Such modification would involve only routine skills in the art, and would result in a smaller size device.

Conclusion

8. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
August 9, 2005